REMARKS

Applicant has carefully studied the outstanding Official Action. The present response is intended to be fully responsive to all points of rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Claims 20, 23, 26-28 and 38 stand rejected under 35 USC 102(b) as being anticipated by Martin. Claims 22 and 34 stand rejected under 35 USC 103(a) as being unpatentable over Martin and further in view of Salatino et al. Claims 24, 33 and 36 stand rejected under 35 USC 103(a) as being unpatentable over Martin and further in view of Ichikawa. Claim 29 stands rejected under 35 USC 103(a) as being unpatentable over Martin and further in view of Malinovich et al.

Martin describes a cover for a micromechanical device through which input/output connections to the device are made. Salatino discloses a wafer level hermetically packaged integrated circuit. Ichikawa discloses a method for manufacturing surface acoustic modules. Malinovich describes a method for producing a back-illuminated CMOS image sensor including a matrix of pixels that are fabricated on a semiconductor substrate.

Applicant has amended claim 20 to recite that the method of the present invention seals at least one chip scale packaging layer onto a semiconductor substrate, producing individual chip scale packaged devices.

Support for the amendments to claim 20 can be found in the disclosure on page 2, lines 18-22.

Applicant respectfully submits that none of the prior art, either alone or in combination shows or suggests a method of producing a crystalline substrate based device including

"adhesively sealing to" a "wafer at least one transparent chip scale packaging layer and" a "spacer onto" a "semiconductor substrate over" a "microstructure and at least partially spaced therefrom, thereby to define at least one gap at . . . at least one cavity between said microstructure and said at least one chip scale packaging layer" and "subsequently dicing said wafer into said individual chip scale packaged devices" as recited in amended claim 20.

Applicant has added new claims 39-67. New claims 39-49, 51-56 and 59-67 are method claims corresponding to allowed apparatus claims 1-26 in parent application 09/725,166, now U.S. Patent 6,777,767. New claims 50, 57 and 58 are method claims similar in scope to allowed apparatus claims 17, 9 and 11 in parent application 09/725,166, now U.S. Patent 6,777,767, respectively.

Applicant has carefully studied the remaining prior art of record herein and concludes that the invention as described and claimed in the present application is neither shown in nor suggested by the cited art.

In view of the foregoing remarks, all of the claims are believed to be in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Respectfully submitted,

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